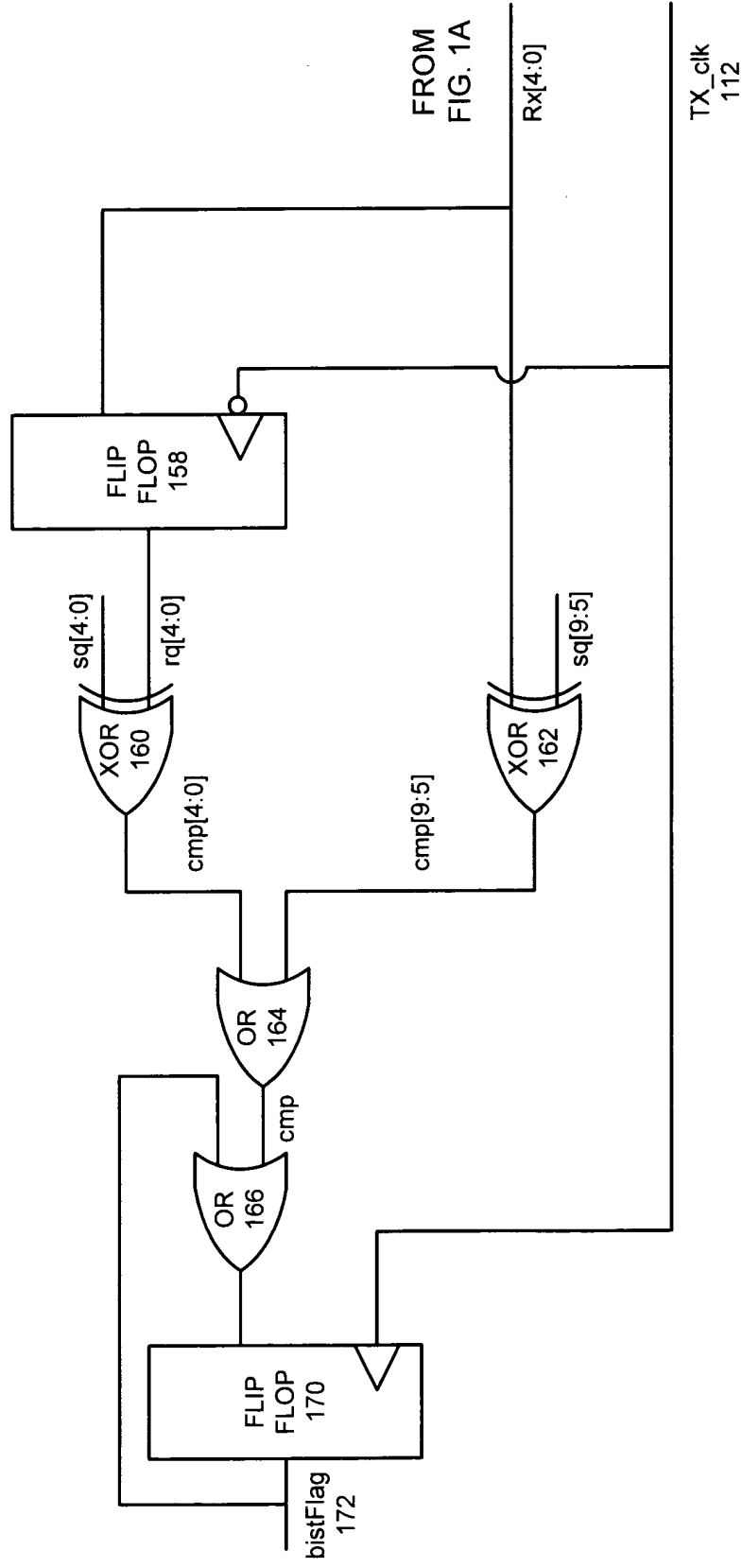
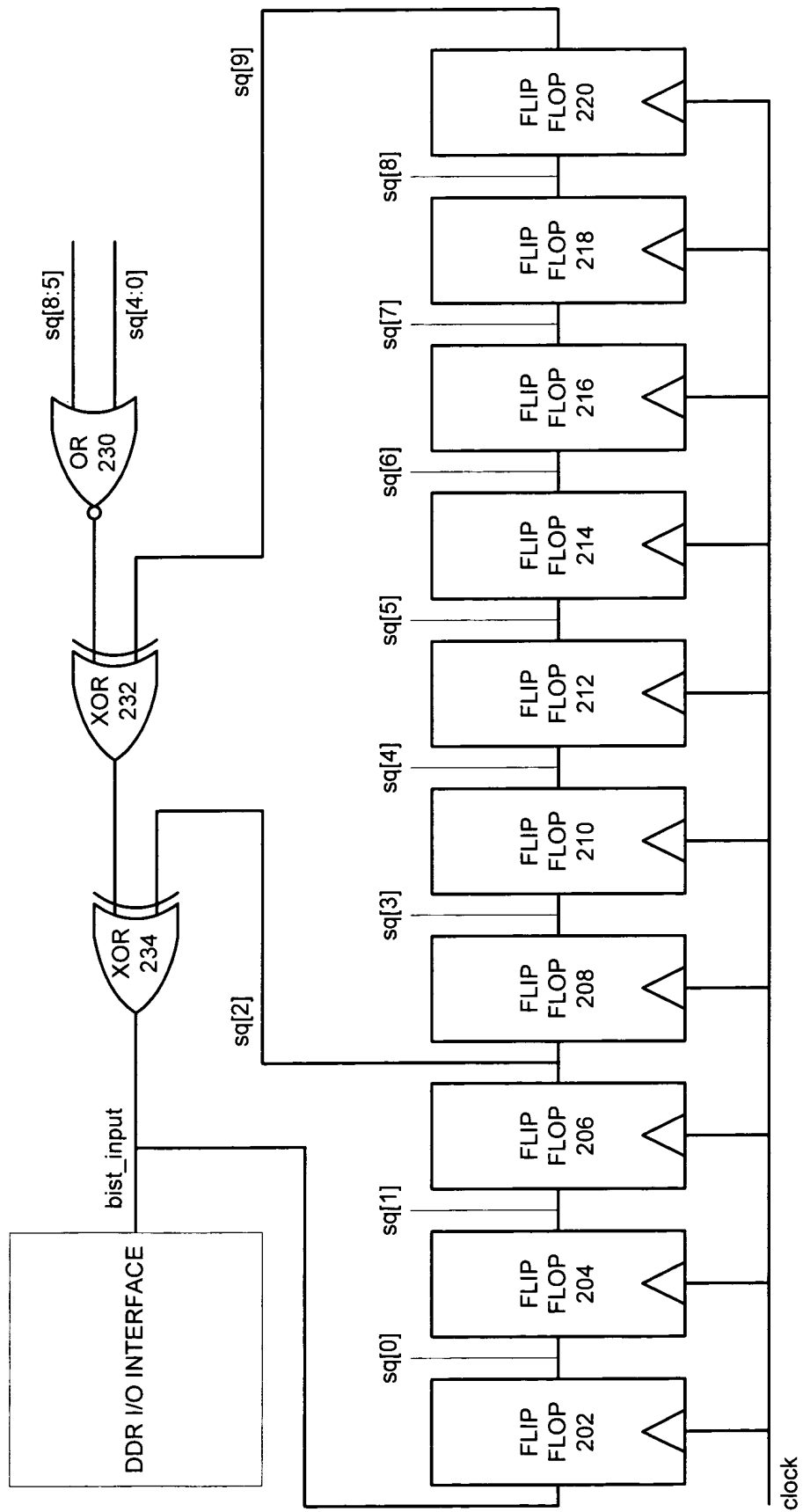


FIG. 1A



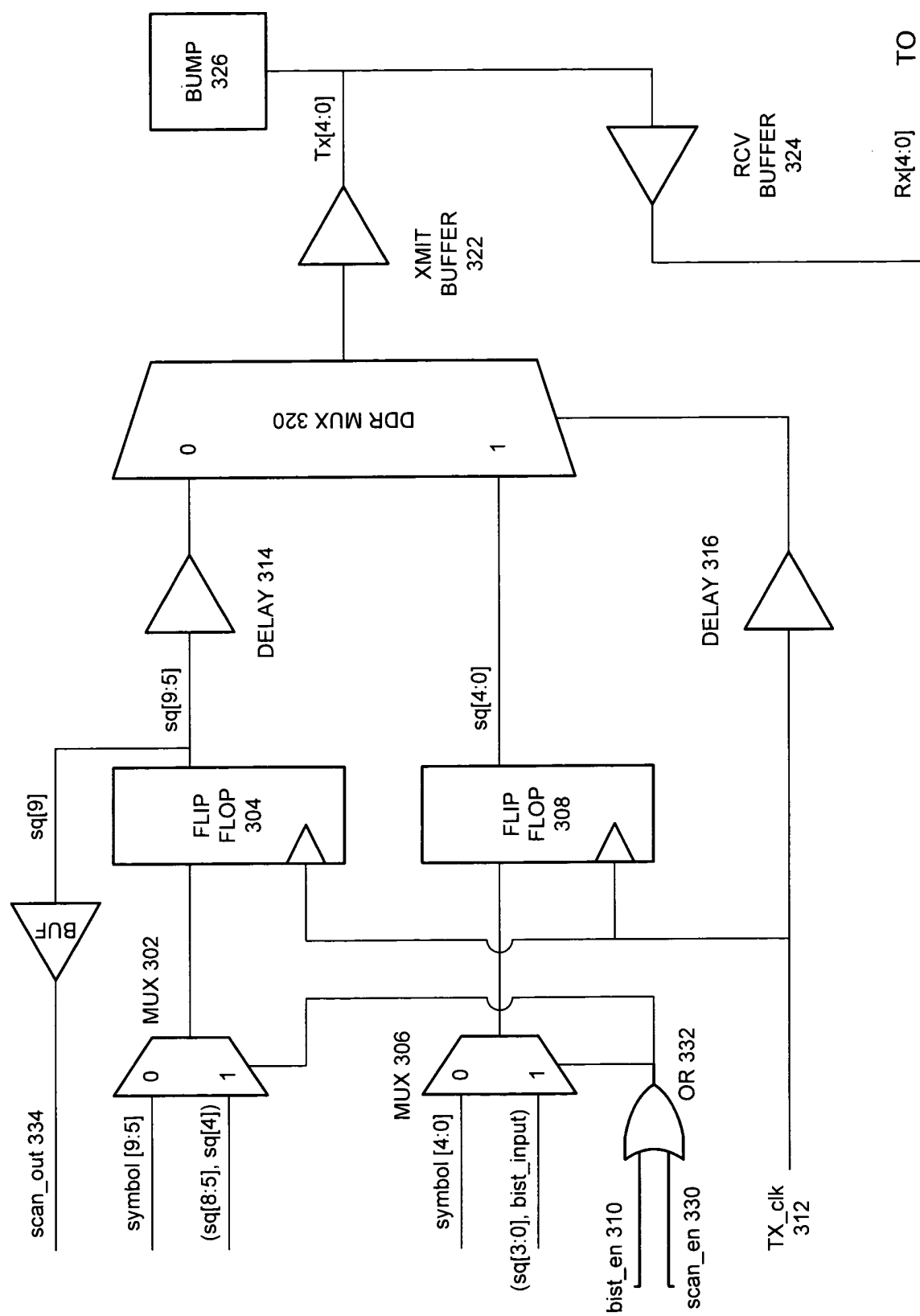
DDR OUTPUT MACRO CELL
100

FIG. 1B



LINEAR FEEDBACK SHIFT REGISTER
200

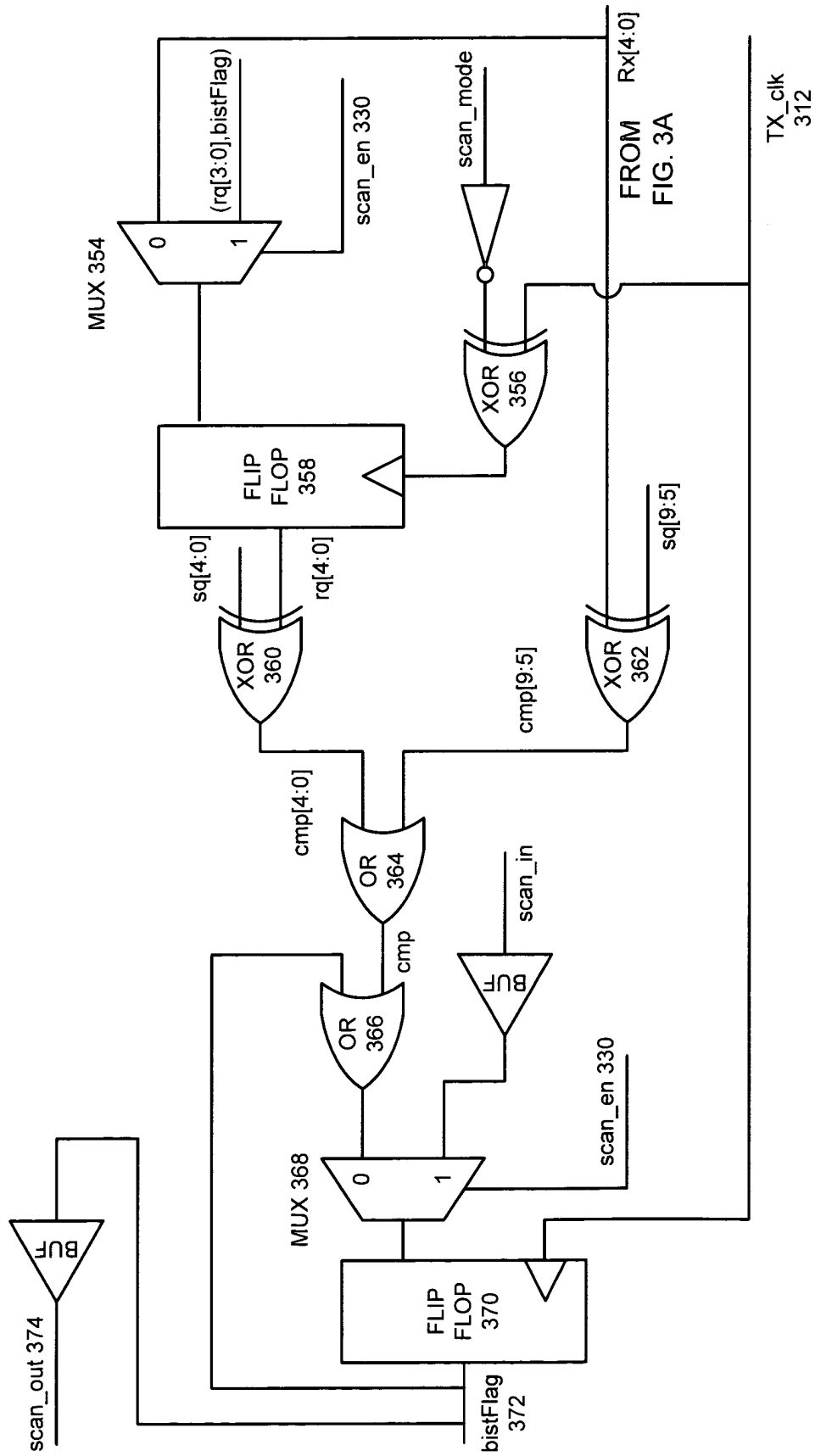
FIG. 2



DDR OUTPUT MACRO CELL 300

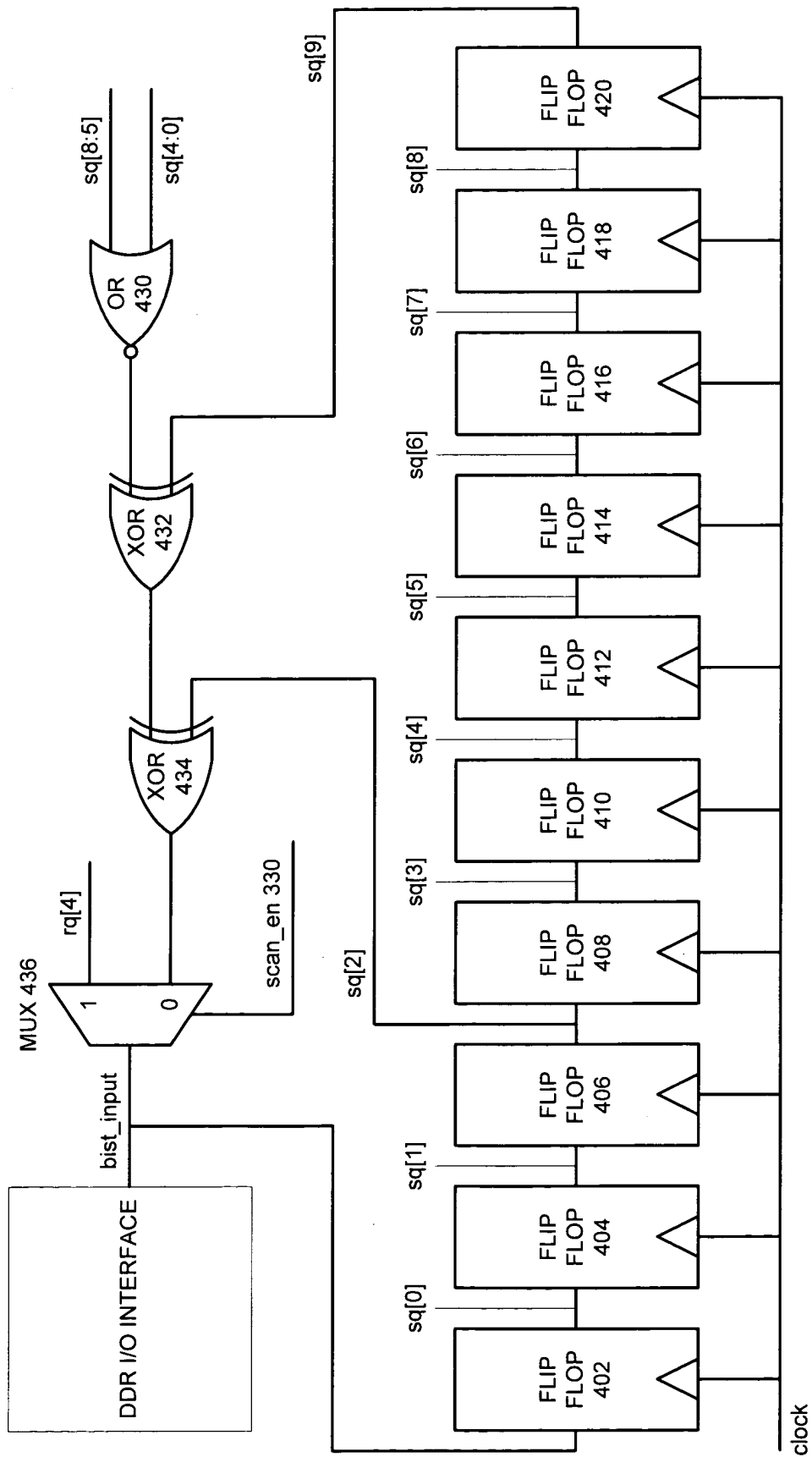
FIG. 3A

TO
FIG. 3B



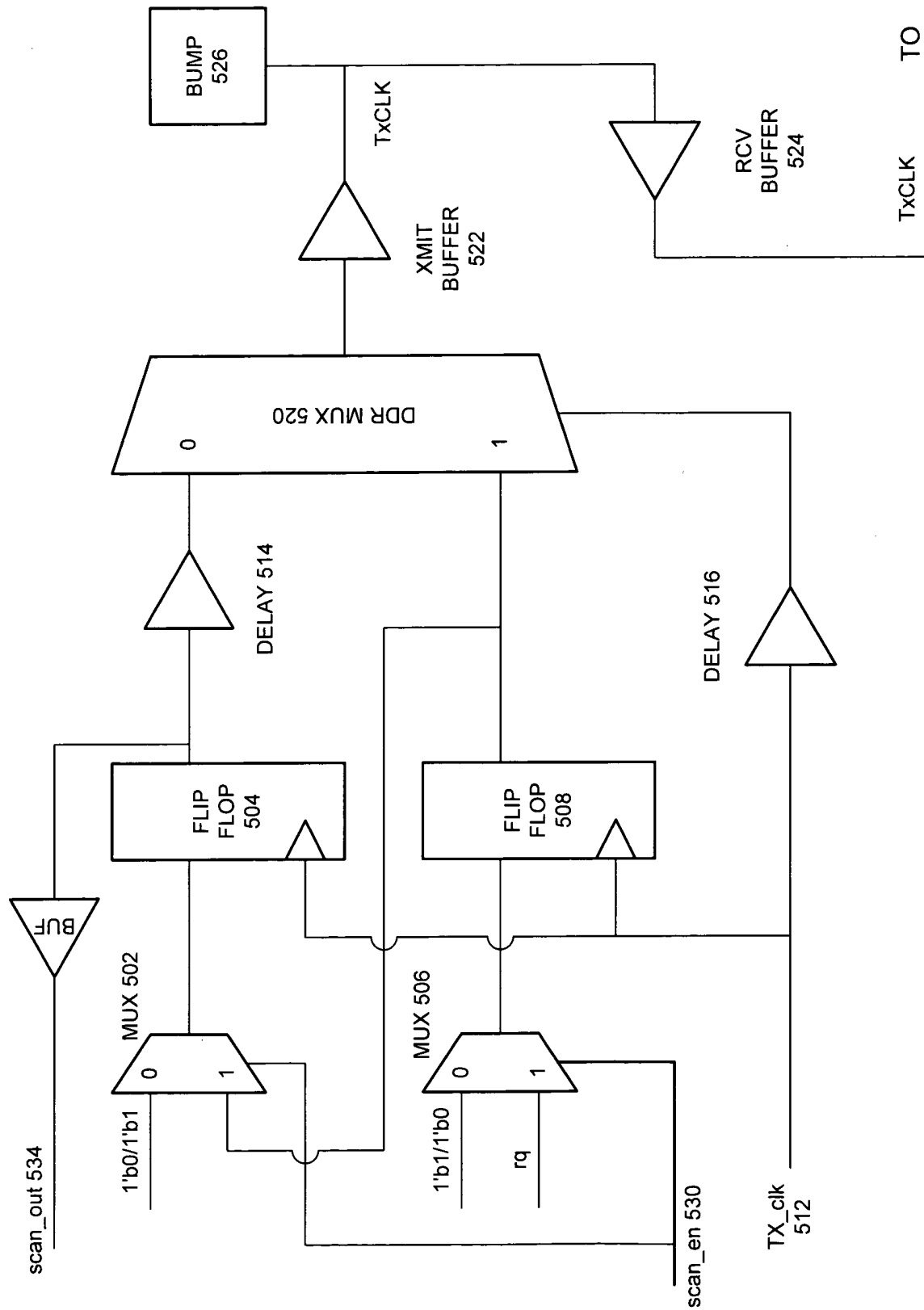
DDR OUTPUT MACRO CELL
300

FIG. 3B



LINEAR FEEDBACK SHIFT REGISTER
400

FIG. 4

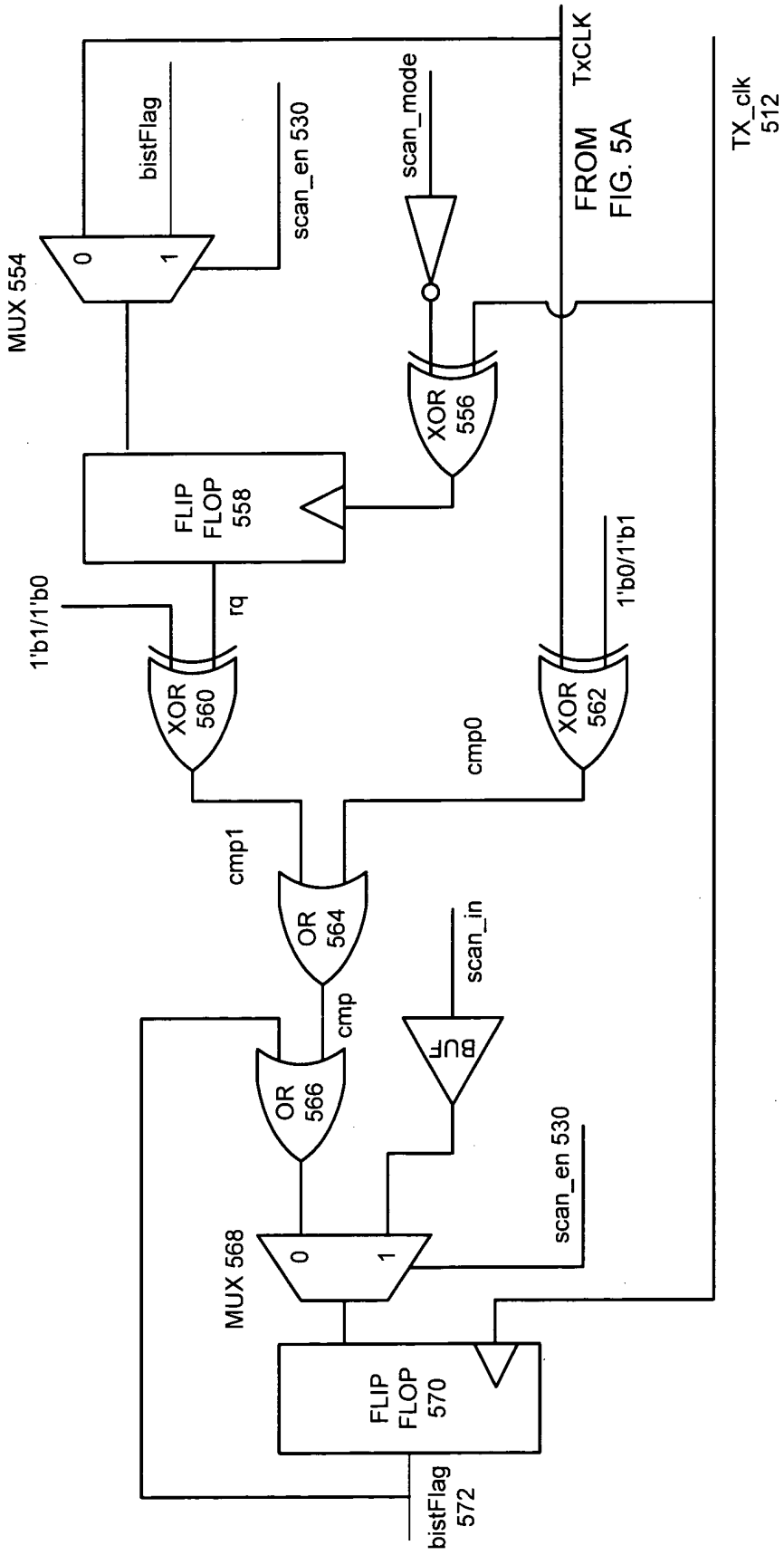


CLOCK OUTPUT MACRO
CELL 500

FIG. 5A

TO
FIG. 5B

SECRET



CLOCK OUTPUT MACRO
CELL 500

FIG. 5B

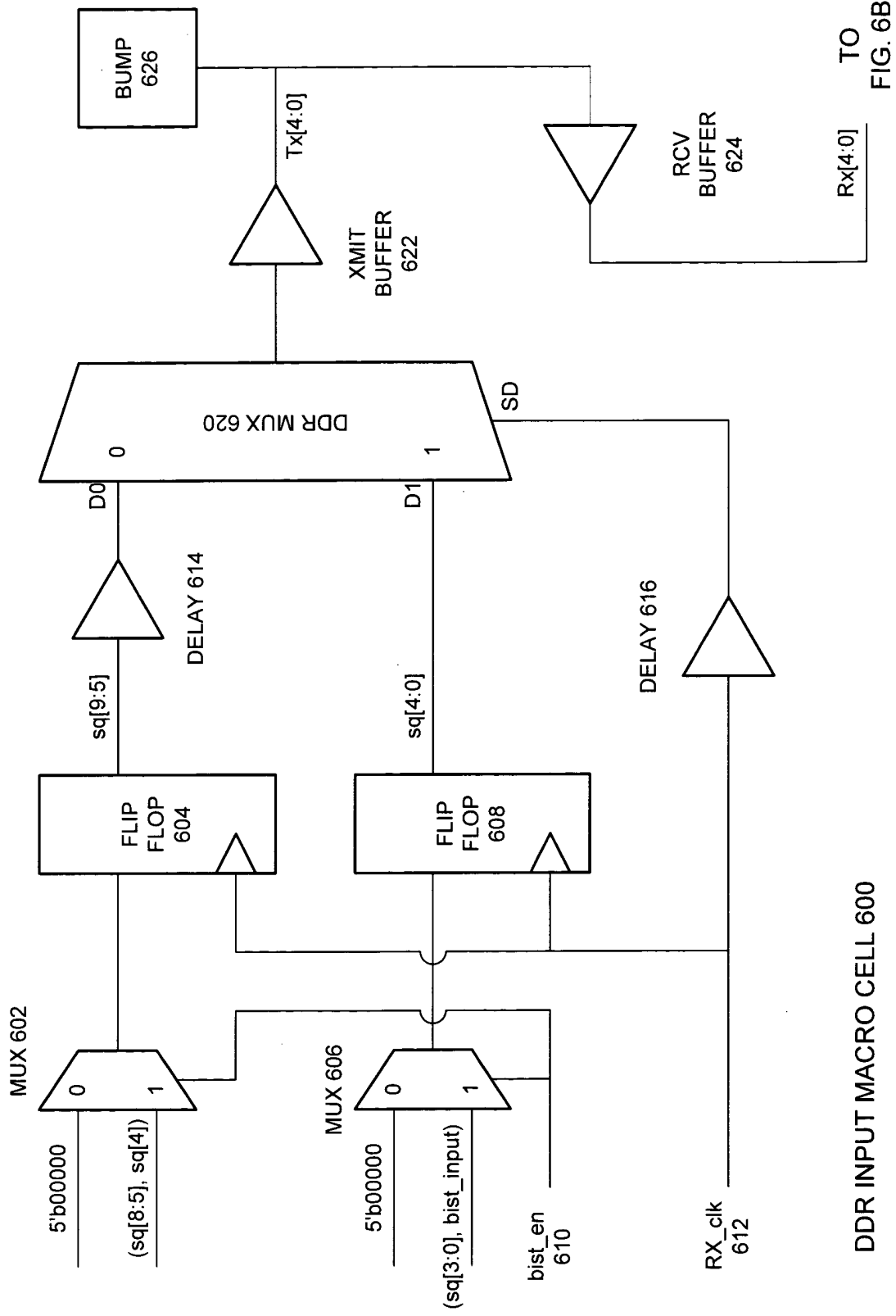


FIG. 6A

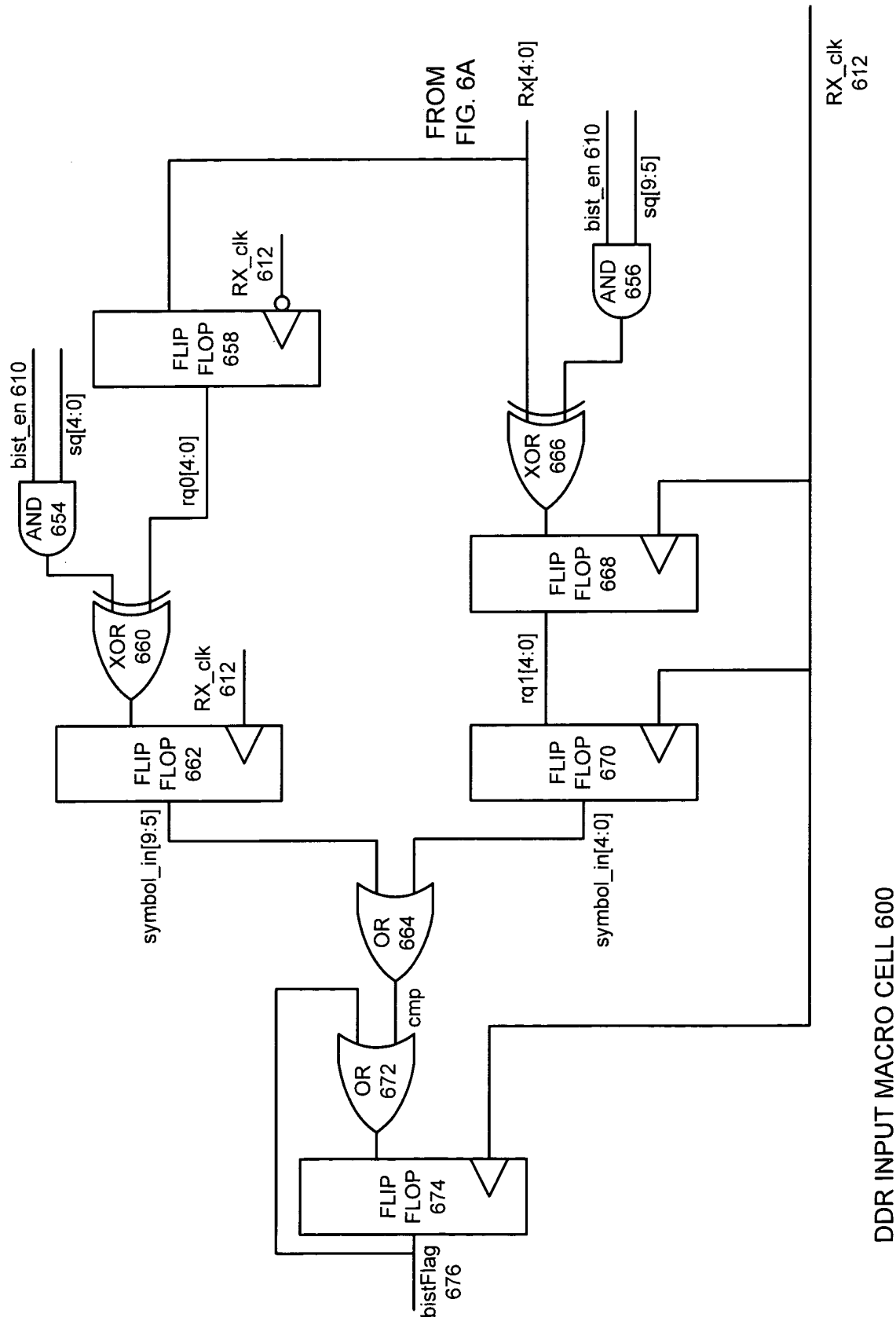
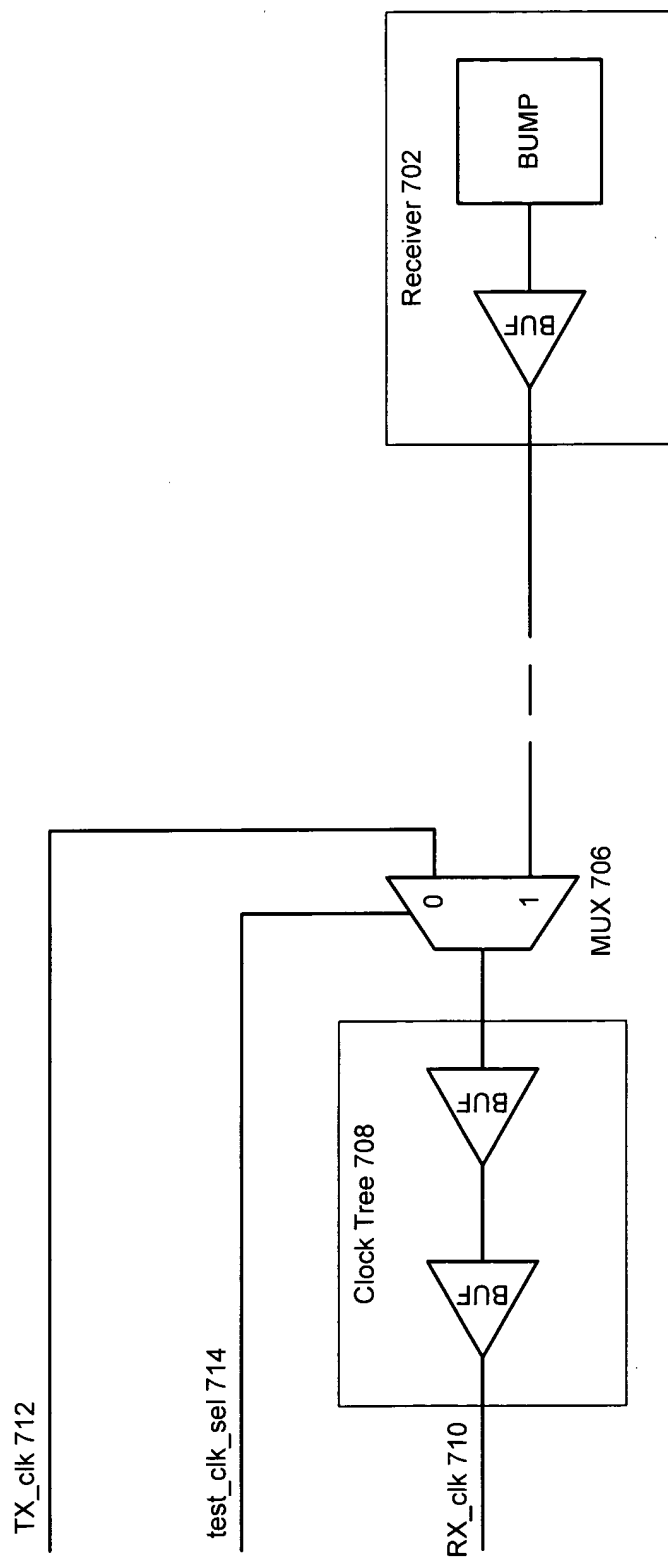


FIG. 6B



CLOCK INPUT MACRO CELL
700

FIG. 7

060905Z JUL 78

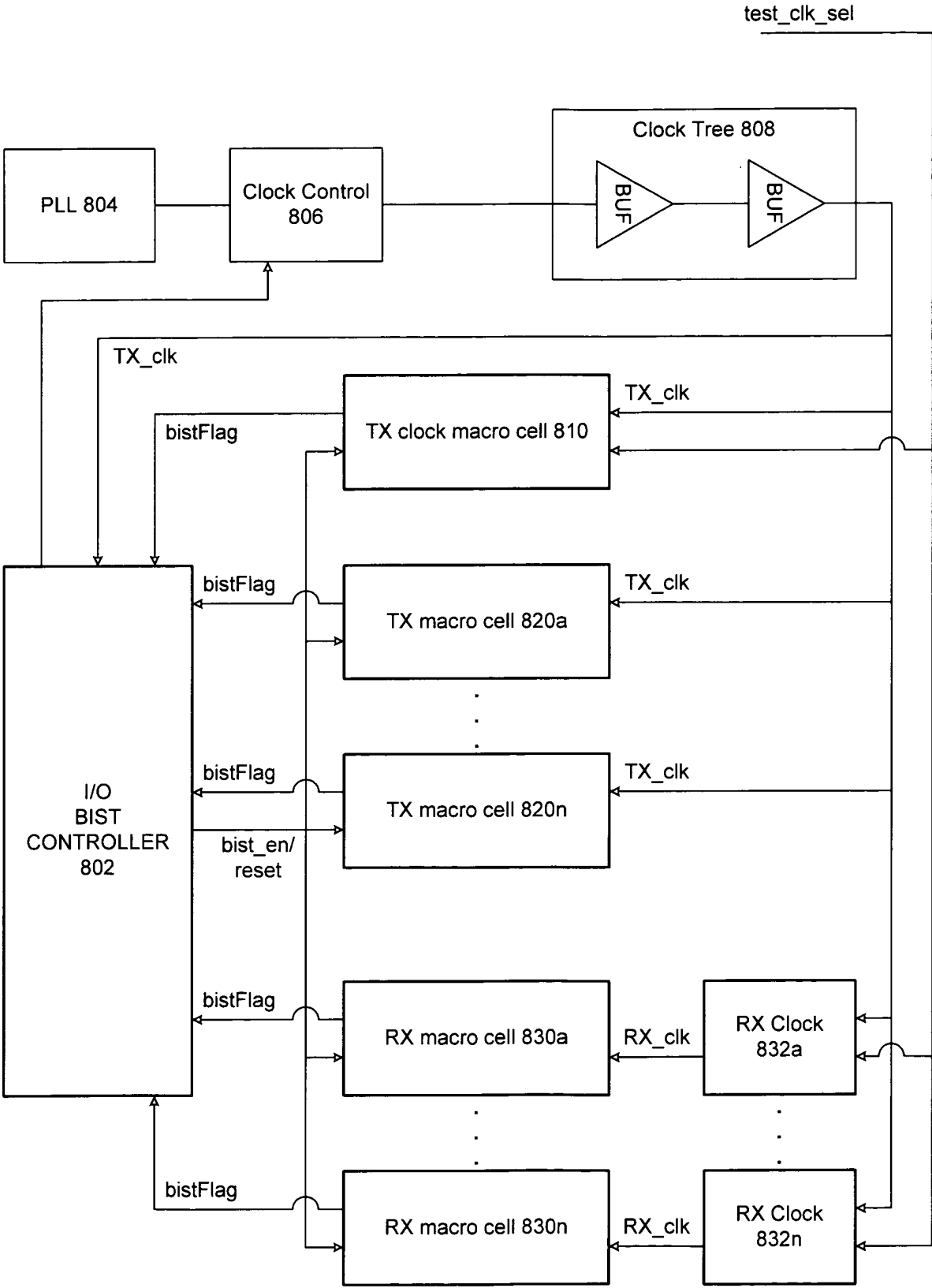


FIG. 8